REMARKS

Claims 1-9, 11, and 16-25 are pending in the present application. Claims 1, 8, 18, and 22 are independent.

Reconsideration and allowance are respectfully requested in view of the following remarks.

Claim Rejection Under 35 U.S.C. § 112

Claims 1-9, 11 and 17 were rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement because a capacitor is not recited in the independent claims. This rejection is respectfully traversed because while a capacitor can be included to provide a bias, such a feature is not necessary to practice the broad invention encompassed by Applicants' independent claims. Moreover, it is well-established in the MPEP that it is the function of the specification, and not the claims, to provide an enabling description for how one skilled in the art is to practice the claimed invention. See, for example, MPEP §§ 2164-2164.01.

An exemplary embodiment of the disclosure provides an amplifier unit including a first amplifier (e.g. transistor 110a) and a second amplifier (e.g. transistor 110b), each of which includes a source (e.g. lowest terminal in Fig. 1), a drain (e.g. highest terminal in Fig. 1), and a gate (e.g. middle terminal in Fig. 1). In the exemplary amplifier unit, the gate of the first amplifier 110a and the gate of the second amplifier 110b are connected to a common gate connection (e.g. the nodes connected to DC feed 120). The drain of the first amplifier 110a and the drain of the second amplifier 110b are connected to a common drain connection (e.g. the nodes

connected to DC feed 130). The drain of the first amplifier 110a is connected to the gate of the second amplifier 110b. See, for example, paragraph 11 of the specification, which provides that exemplary embodiments can include a DC feed 130 that provides a bias on the drain of transistors 110a, 110b, and 110c.

Claim 1 recites that the drain of the first amplifier is connected to the gate of the second amplifier, and broadly encompasses features of the above discussed embodiments. Claim 5 recites that the drain of the second amplifier is connected to the gate of the third amplifier (e.g. transistor 110c in Fig. 1), and also broadly encompasses features of the above-discussed embodiments.

In rejecting claims 1-9, 11, and 17 under 35 U.S.C. § 112, first paragraph, the Examiner alleged that "[t]he specification states that a capacitor is [needed] to prevent any DC bias current. The Examiner believes that without the involving of the capacitor, the circuit is not enabled." This assertion is not supportable and is contrary to the actual disclosure of the specification. It is instructive to note that the Examiner did not provide any citation to the specification for his belief that a capacitor is needed. DC capacitors 125a, 125b, 125c are shown in Fig. 1, which illustrates an exemplary embodiment of the invention. Fig. 1 is described, for example, in paragraph [0011] of the specification. In this description, the DC blocking capacitors are not described as essential for practice of the invention. On the other hand, according to an exemplary embodiment described above, the DC feed 30, for example, provides a bias on the drain of the transistors 110a, 110b, 110c. As such, contrary to the Examiner's unfounded interpretation, the specification does not require the provision of capacitors to prevent any DC bias current. Therefore, the claims do not lack essential subject matter as alleged by the Examiner.

Accordingly, Applicants' claims are enabled by the original disclosure, which reasonably conveys to one skilled in the relevant art how to make and use embodiments of the claimed invention without undue experimentation. Withdrawal of the rejection under 35 U.S.C. § 112 is therefore respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-5, 7, 8 and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Turlington et al. (U.S. Patent No. 5,940,031 A1) in view of Khorram (U.S. Patent No. 7,088,969 B2) and Duffalo (U.S. Patent No. 4,890,069). On page 7 of the Office Action, claims 6, 11 and 17 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Turlington, Duffalo and Khorram in view of Saxler (U.S. Patent No. 7,030,428 B2). Later on page 7, claims 18-25 are rejected as being unpatentable over Khorram in view of Duffalo. These rejections are respectfully traversed.

The Examiner acknowledges that Turlington and Saxler do not disclose an amplifier unit, as recited in any of independent claims 1, 8, 18, and 22. In striving to remedy this deficiency, the Examiner alleges that Khorram and Duffalo can be combined to form the recited amplifier units. This assertion is unsupportable, as one skilled in the art would have no reason to combine Khorram and Duffalo to result in the amplifier units of claims 1, 8, 18, and 22.

In Fig. 9 of Khorram, a highly linear power amplifier 212 is illustrated.[1] The power amplifier 212 includes an input signal 236 and an output 240. The amplifier 212 of Khorram includes a number of transistor pairs 224, 226, 228. Each transistor

[1] The discussion of the amplifier 212 of Khorram focuses on the upper portion of the amplifier 212 connected to component 220, but it also applies to the lower portion of the amplifier 212 connected to component 222.

pair 224, 226, 228 includes an enable transistor and an input transistor. The gates of the input transistors are commonly coupled to the input signal 236. The enable transistors are coupled to individual enable signals 244, 246, 248. The enable signals 244, 246, 248 enables any combination of the input transistors to be coupled to the output 240 so as to produce a desired gain for the power amplifier 212.

In contrast to Khorram, Duffalo discloses a preamplifier (Fig. 1) that is not disclosed as linear, and, as illustrated in Fig. 2 (see the certificate of correction of Duffalo), the preamplifier has varying gain depending on the frequency of the input signal. The preamplifier of Duffalo consists of three stages: matching circuit 30; class A gain stage 40; and class B gain stage 50. As illustrated in Fig. 1 of Duffalo, N-channel FET 44, which is part of class A gain stage 40, is coupled to open drain FET 54 of class B stage 50 via blocking capacitor 51.

The Examiner alleges that it would have been obvious to combine Duffalo and Khorram to "properly supply DC bias current to the gate of the second amplifier." Applicant respectfully submits that this is not a valid reason to combine the documents in any manner, and in particular not in the manner of independent claims 1, 8, 18, and 22. On page 8 of the Office Action, in rejecting claim 19, the Examiner alleges that DC blocking capacitor 51 of Duffalo is present in the combination and is connected to a "second amplifier" 54. Since the capacitor 51 blocks DC current, using the DC blocking capacitor of Duffalo would not achieve the Examiner's reason for the proposed combination of supplying DC bias current to the gate of the second amplifier.

Other than the Examiner's conclusory assertion, there is no reason why one skilled in the art would attempt the alleged combination to arrive at a functioning

linear, multiple stage power amplifier. Khorram and Duffalo both disclose amplifiers with unique structures and different transfer characteristics, precluding one skilled in the art from having had a reason to modify the documents in the combination alleged by the Examiner. The Examiner's proposal to modify the interconnections of the transistors which make up the building blocks of Khorram and Duffalo would result in wholly different circuitry from the individually disclosed amplifiers of Khorram and Duffalo.

It is unclear as to exactly how the Examiner is proposing to combine the disclosures of Khorram and Duffalo. If the Examiner is to continue to attempt to combine Khorram and Duffalo in rejecting the application, Applicant respectfully requests further clarification as to whether Duffalo is being modified with features of Khorram or whether Korram is being modified with features of Duffalo, what the resulting circuit would look like, and how it might "properly supply DC bias current to he gate of the second amplifier". What does the Examiner consider to be the second amplifier in the combination? Moreover, what does the Examiner consider to be the third amplifier or third transistor, as recited in claims 5, 21, and 25?

It is improper to combine bits and pieces of incongruous references in an attempt to arrive at the subject of a claim without a reasonable motivation for doing so. Furthermore, in proposing to combine two wholly different amplifiers in a manner that is not even apparently able to be articulated, other than in an attempt to arrive at the claimed invention. The Examiner must demonstrate with appropriate technical reasoning why such a theorized modification could predictably lead one skilled in the art to combine the various bits and pieces of the applied references to arrive at the claimed invention. See MPEP 2143(a).

Turlington, Duffalo, Saxler, and Khorram, whether considered alone or in the combination set forth by the Examiner, do not disclose all of the features of claims 1, 8, 18, and 22. Accordingly, these claims are allowable. Dependent claims 2-7, 9, 11, 16, 17, 19-21, and 23-25 are allowable by virtue of their dependency from allowable claims 1, 8, 18, and 22 and on their own merits. For example, the alleged combination does not disclose a third amplifier or third transistor, as recited in claims 5, 21, and 25.

Conclusion

From the foregoing, further and favorable action in the form of a Notice of Allowance is respectfully requested.

In the event that there are any questions concerning this amendment, or the application in general, the Examiner is respectfully requested to telephone the undersigned so that prosecution of present application may be expedited.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

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By: _____ #63985
Patrick C. Keane
Registration No. 32858

Customer No. 21839
703 836 6620